MANUFACTURABLE TRI-STACK ALSB/INAS HEMT LOW-NOISE AMPLIFIERS USING WAFER-LEVEL-PACKAGING TECHNOLOGY FOR LIGHT-WEIGHT AND ULTRALOW-POWER APPLICATIONS

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***Abstract*—A wafer-level-packaging technology was used to integrate the 0.1 μm AlSb/InAs HEMT low-noise amplifiers with power amplifiers, switches and phase shifters to form a compact tri-stack transmit/receive module for light-weight and ultralow-power applications. The high manufacturability of AlSb/InAs HEMT receivers operating at 0.9 mW was demonstrated on a tri-stack wafer. This demonstration of manufacturable tri-stack transmit/receive modules is essential for phased-array applications requiring light weight and ultralow power.**

Keywords-wafer-level-packaging; HEMT; ultralow-power; AlSb/InAs;

I. INTRODUCTION

The AlSb/InAs HEMT has proven to be a viable next-generation transistor for ultralow-power, low-noise, and high-speed applications due to the superior electronic properties of the InAs channel, such as electron mobility and peak electron velocity [1]-[4]. The electron mobility and peak electron velocity are nearly two times larger than those of InGaAs-channel InAlAs/InGaAs/InP HEMTs [5]. For metamorphic InAs-channel AlSb/InAs HEMTs, the combinations of high peak electron velocity (~ $4x10^7$ cm/s) at low electric field, and high channel conductivity, enable operation at very low drain voltage (V_{DS} < 0.2 V). As a result, AlSb/InAs HEMTs have demonstrated 5 to 10 times lower power dissipation than conventional InP HEMTs and metamorphic HEMTs [6]-[8]. Accordingly, AlSb/InAs HEMTs have become important components for phased-array applications requiring ultralow power [6].

On the other hand, the design of a phased-array system is power constrained. With the quantities of low-noise amplifiers (LNAs) used in a phased-array system up to 10^6, reduction of power dissipation becomes a big challenge. A decrease of dc power dissipation in LNAs from 15 mW to 0.9 mW would result in a dc power reduction on the order of 14 kW. Additionally, Northrop Grumman Corporation (NG) has developed a wafer-level-packaging (WLP) technology for multi-layer GaAs monolithic-microwave-integrated-circuit (MMIC) integration [9-10]. For the first time, WLP technology was used to integrate AlSb/InAs HEMT LNAs with other elements to form a tri-stack transmit/receive module (TRM). In this paper, the high manufacturability of AlSb/InAs HEMTs operating at 0.9 mW is demonstrated on a tri-stack wafer. This demonstration of manufacturable tri-stack TRMs is essential for phased-array applications requiring light weight and ultralow power.

II. AlSb/InAs HEMTs

The AlSb/InAs HEMT structure shown in Fig. 1 was grown by molecular-beam epitaxy (MBE) on 3-inch semi-insulating GaAs substrates. AlGaSb was used as a buffer. AlSb was used as an electron barrier, and $In_{0.4}Al_{0.6}As$ was used as a hole

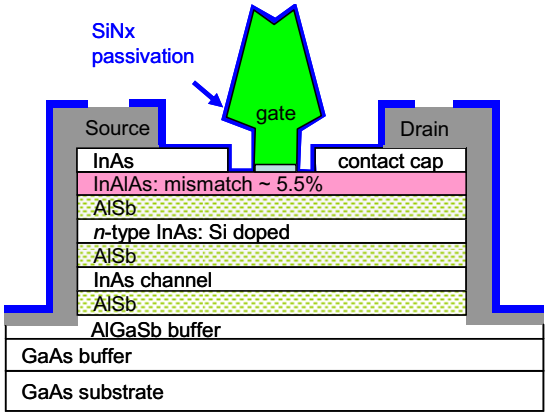

Figure 1: Cross section of an AlSb/InAs HEMT device on a 3-inch GaAs substrate. The interface region between the $In_{0.4}Al_{0.6}As$ barrier and gate metallization is critical for high device yield.

barrier. Silicon-doped InAs was used to supply electrons to the InAs channel. Detailed information regarding the design of this structure can be found in previous publications [2], [11]. Note that the lattice mismatch of the $In_{0.4}Al_{0.6}As$ barrier to the underlying AlSb barrier is as high as 5.5%. Because the $In_{0.4}Al_{0.6}As$ relaxes, its thickness is only grown to 40 Å in this device structure in order to minimize its impact on material quality. The relaxation and thinness of this layer results in stronger dependence of performance and manufacturability of AlSb/InAs HEMTs on gate metallizations due to their interaction with the $In_{0.4}Al_{0.6}As$. Therefore, TiW has been used as gate metallization on our AlSb/InAs HEMTs for high manufacturability [12].

The typical current-voltage characteristics of a 0.1 µm AlSb/InAs HEMT is shown in Fig. 2, illustrating the advantages of AlSb/InAs HEMTs with low V_{DS} operation, low knee voltage (V_K), low on-resistance (R_{ON}) and high transconductance (g_m), which are important for ultralow-power and high-frequency applications. Typically, devices exhibit a low-field R_{ON} at V_{GS}=0V of approximately 0.55 Ω mm. The peak g_m at V_{DS} = 0.2 V is approximately 1,000 mS/mm. The non-pinch-off drain current (I_{DS}) at V_{DS} = 0.2 V and V_{GS} = -1 V is as low as 2 mA/mm. The in-line dc functional yield of AlSb/InAs HEMTs is as high as 95%, showing that a manufacturable AlSb/InAs HEMT technology has been achieved at NG. Additionally, the current gain and unilateral gain as a function of frequency were measured on a 4×200 AlSb/InAs HEMT device biased at V_{DS} = 0.15 V and V_{GS} = -0.3 V. Extrapolated values for unity-current-gain cut-off frequency, f_T, of 147 GHz, and maximum frequency of oscillation, f_{MAX}, of 110 GHz, were obtained. This demonstrates the benefits of AlSb/InAs HEMTs for ultralow-power and high-frequency applications.

III. Tri-stack Transmit/Receive Modules

Figure 3 shows the cross section of a tri-stack WLP transmit/receive module. The required components from different technologies were processed separately. The AlSb/InAs HEMT low-noise amplifiers were processed on the bottom 3" wafer. The other components of power amplifiers, switches, and phase shifters were processed on the middle and

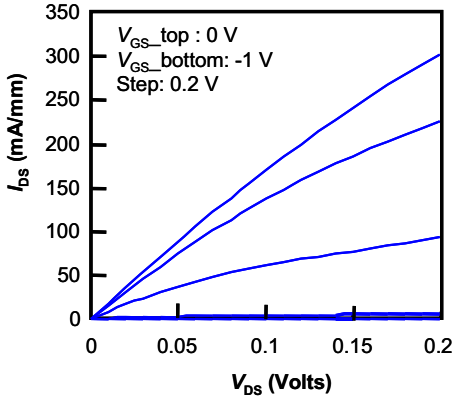

Figure 2: Current-voltage characteristics of a 0.1 µm AlSb/InAs HEMT.

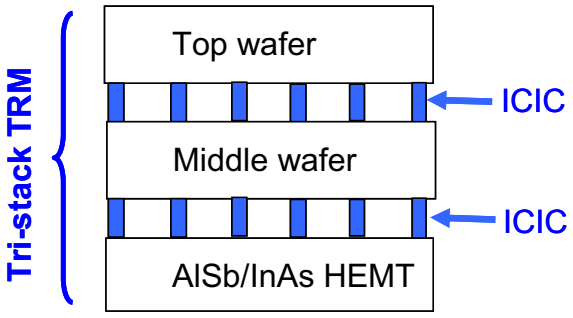

Figure 3: Cross section of a tri-stack transmit/receive module. The AlSb/InAs HEMT LNA resides on the bottom of this tri-stack WLP module.

top 4" wafers. After completing the front-side processes of each individual wafer, an intracavity interconnection (ICIC) metallic layer was deposited on the wafers. Then, the bonding layer was deposited on top of the ICIC layer of these three wafers to facilitate the subsequent bonding process to integrate these wafers together. Our low-temperature WLP process activates the bonding layer and fuses together the ICIC layer on these three wafers [10]. The low-temperature WLP process prevents devices from degradation during the process. Detailed information of WLP processes can be found in previous publications [9-10].

Figure 4 shows the scanning-electron micrograph (SEM) of a tri-stack WLP wafer using GaAs and InP mechanical wafers. The results show that our WLP processes are compatible among different technologies to fabricate and integrate AlSb/InAs LNAs, power amplifiers, switches, and phase shifters to form a tri-stack TRM.

Additionally, an x-ray computed tomography (XCT) technique was used to check the ICIC integrity on a tri-stack TRM. Figure 5 shows an XCT image of a tri-stack TRM with good ICIC integrity (no open or short). The test elements for ICIC integrity on wafers after bonding were also measured to verify ICIC integrity. Typically, the ICIC electrical yield of a tri-stack wafer is greater than 90%. This suggests that a high-yield process has been achieved on NG's WLP technology. This is essential for manufacturable WLP technology to fabricate tri-stack TRMs.

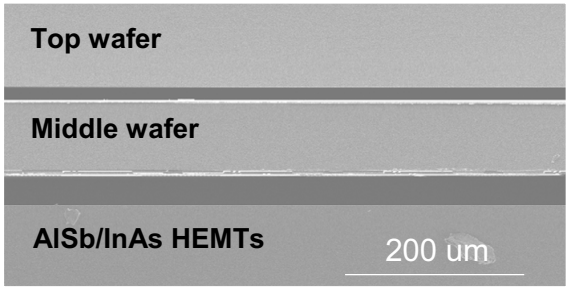

Figure 4: SEM micrograph of a tri-stack WLP wafer. This was demonstrated using mechanical wafers.

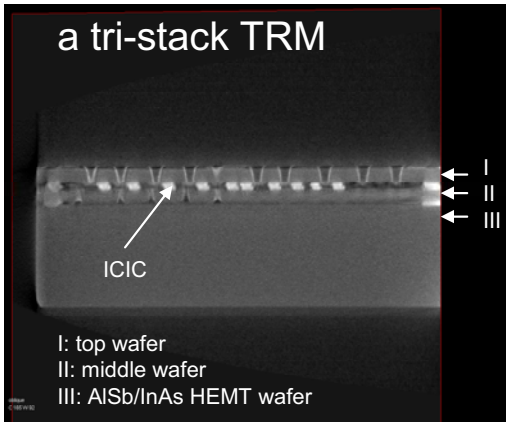

Figure 5: X-ray computed tomography of a complete tri-stack TRM. It shows good ICIC integrity among these three wafers.

IV. TRI-STACK AlSb/InAs HEMT LNAs

Figure 6 shows the top view of two complete tri-stack transmit/receive modules. Each compact module contains AlSb/InAs LNAs, power amplifiers, switches, and phase shifters. This module has weight below 24 mg and size of 5 mm^2, showing significant reduction of weight and size of transmit/receive modules as compared to conventional transmit/receive modules. This demonstration of compact and low-weight transmit/receive modules is crucial for phased-array applications requiring millions of transmit/receive modules.

In our tri-stack transmit/receive modules, power amplifiers, switches, and phase shifters were fabricated using mature GaAs and InP technologies. As a result, the manufacturability of AlSb/InAs HEMT LNAs is the key to having high-yield demonstration of a tri-stack WLP technology. After forming a tri-stack wafer, on-wafer radio-frequency (rf) testing was performed to measure the rf performance of ASb/InAs LNAs, power amplifiers, switches, and phase shifters. Generally, the rf yield and performance of power amplifiers, switches, and phase shifters is comparable with that of power amplifiers, switches, and phase shifters without WLP processes. This shows that our WLP processes do not introduce negative factors to affect RF yield and performance of power amplifiers, switches, and phase shifters.

Figure 6: Top view of a light-weight and compact TRM, with weight < 24 mg and size of 5 mm^2.

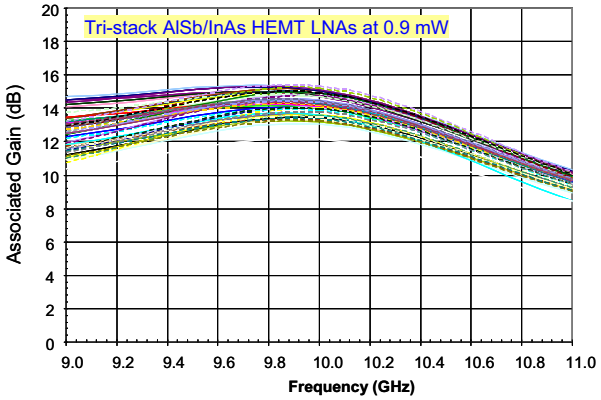

Figure 7: Associated gain distribution across a 3-inch tri-stack wafer of AlSb/InAs HEMT LNAs operating at P_{DC} of 0.9 mW (V_{DS} = 0.15 V and I_{DS} = 6 mA).

Figure 7 shows the on-wafer rf performance of AlSb/InAs HEMT LNAs on a tri-stack WLP wafer. The LNAs were designed for X-band applications, and biased at V_{DS} = 0.15 V and I_{DS} = 6 mA, with power dissipation (P_{DC}) of 0.9 mW. The histograms of associated gain (Ga) and noise figure (nf) of AlSb/InAs HEMT LNAs operating at P_{DC} of 0.9 mW and frequency of 10 GHz are shown in Figs. 8 and 9. The average Ga and nf, which include the loss due to switches and phase shifters in a TRM, are approximately 13 and 3.5 dB, respectively. The results achieved here demonstrate a manufacturable tri-stack process for AlSb/InAs HEMT low-noise amplifiers using wafer-level-packaging technology for light-weight and ultralow-power applications.

V. CONCLUSIONS

A wafer-level-packaging technology was used to integrate 0.1 μm AlSb/InAs HEMT low-noise amplifiers with power amplifiers, switches and phase shifters to form a compact tri-stack transmit/receive module for light-weight and ultralow-

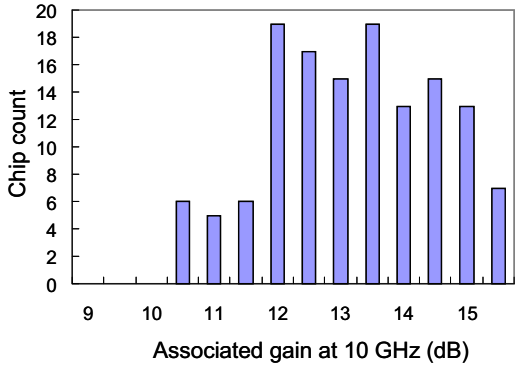

Figure 8: Histogram of associated gain distribution across a 3-inch tri-stack wafer of AlSb/InAs HEMT LNAs operating at P_{DC} of 0.9 mW (V_{DS} = 0.15 V and I_{DS} = 6 mA).

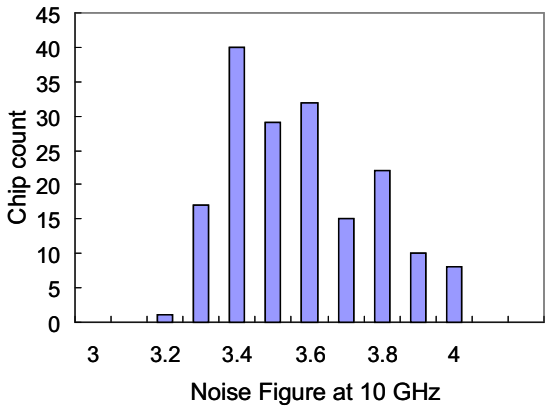

Figure 9: Histogram of noise figure distribution across a 3-inch tri-stack wafer of AlSb/InAs HEMT LNAs operating at P_{DC} of 0.9 mW (V_{DS} = 0.15 V and I_{DS} = 6 mA).

power applications. The complete module has weight below 24 mg and size of 5 mm^2. For the first time, manufacturable AlSb/InAs HEMT receivers operating at 0.9 mW were demonstrated on a tri-stack wafer using WLP technology. This accomplishment of compact tri-stack transmit/receive modules is crucial for phased-array applications with light-weight and ultralow-power requirements.

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